What is claimed is:

1. In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of simulation processors;

a first reconfigurable interconnect stage configurable to receive outputs from the simulation processors;

a second reconfigurable interconnect stage configurable to receive outputs from the first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage configurable to receive outputs from the second reconfigurable interconnect stage, and further configurable to provide outputs to inputs of the second reconfigurable interconnect stage.

2. The reconfigurable interconnect network of claim 1, wherein the second reconfigurable interconnect stage is further configurable to provide outputs to inputs of the simulation processors.

3. The reconfigurable interconnect network of claim 1, further including a memory coupled to the second reconfigurable interconnect stage, the second reconfigurable interconnect stage being dynamically configured in accordance with a content of the memory.

4. In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of clusters, each cluster including:

a plurality of simulation processors, and

a first reconfigurable interconnect stage configurable to receive outputs from the simulation processors in the cluster;

a second reconfigurable interconnect stage configurable to receive outputs from the first reconfigurable interconnect stages; and

a third reconfigurable interconnect stage configurable to receive outputs of the second reconfigurable interconnect stage and to provide outputs back to inputs of the second reconfigurable interconnect stage.

5. The reconfigurable interconnect network of claim 3, wherein the second reconfigurable interconnect stage is further configurable to provide outputs back to inputs of the simulation engines of the clusters.

6. In a logic simulation system, a reconfigurable interconnect network comprising:

a first reconfigurable interconnect stage;

a second reconfigurable interconnect stage configurable to receive outputs from the first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage configurable to receive outputs from the second reconfigurable interconnect stage and provide outputs back to the second reconfigurable interconnect stage.

7. The reconfigurable interconnect network of claim 6, wherein the first reconfigurable interconnect stage is coupled to outputs from a plurality of simulation processors.

8 In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of simulation processors;

a first reconfigurable interconnect stage having inputs coupled to outputs of the simulation processors;

a second reconfigurable interconnect stage having inputs coupled to outputs of the first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage having inputs coupled to outputs of the second reconfigurable interconnect stage and outputs coupled to inputs of the second reconfigurable interconnect stage.

9. The reconfigurable interconnect network of claim 8, wherein the outputs of the second reconfigurable interconnect stage are coupled to the inputs of the third reconfigurable interconnect stage using a butterfly topology.

10. The reconfigurable interconnect network of claim 8, wherein the second and third reconfigurable interconnect stages are each a plurality of crossbars.

11. In a reconfigurable interconnect network of a logic simulation system, a method comprising the following steps in the following order:

receiving an output from a first simulation processor;

first routing the output through a first reconfigurable interconnect stage;

second routing the output through a second reconfigurable interconnect stage;

third routing the output back through the first reconfigurable interconnect stage; and

fourth routing the output to a second simulation processor.

12. The method of claim 11, further including a step of, prior to the step of first routing, routing the output from the first simulation processor through a third reconfigurable interconnect stage.

13. The method of claim 11, further including steps of:

first configuring the first reconfigurable interconnect stage, prior to the step of first routing, according to a first configuration; and

second configuring the first reconfigurable interconnect stage, prior to the step of third routing and after the step of first routing, according to a second configuration.

14. In a multi-stage reconfigurable interconnect network of a logic simulation system, a method comprising routing an output from each of a plurality of simulation processors through N physical reconfigurable interconnect stages so as to effectively provide a data path for each output having greater than N reconfigurable interconnect stages.